GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT
COURSE CURRICULUM

Course Title: Computer Organization and Architecture
(Code: 3340705)

Diploma Programmes in which this course is offered	Semester in which offered
Computer Engineering	**4th Sem**

1. RATIONALE

This course provides detail of computer system's functional components, their characteristics, performance and interactions including system bus, different types of memory and input/output organization and CPU. This course also covers the architectural issues such as instruction set program and data types. On top that, the students are also introduced to the increasingly important area of parallel organization. This subject serves as a basic to develop hardware related projects.

2. COMPETENCY

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competency:

- Define and explain computer architecture and organization concept including functional components and their characteristics, performance and the detailed interactions in computer system including system bus, different types of memory and input/output as well as CPU.
- Apply computer architecture theory to solve the basic functional computer problem.
- Show and assemble basic computer components.

3. Course Outcomes:

1.Describe the organization of a computer system in terms of its main components.

2.Identify various parts of a system memory hierarchy.

3.Interface digital circuits to microprocessor systems.

4.Relate design principles in instruction set design including RISC architectures.

4. Teaching and Examination Scheme

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	ESE	PA	ESE	PA	100
3	0	0	3	70	30	00	00	

Legends: L-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** - Practical; **C** – Credit **ESE** - End Semester Examination; **PA** - Progressive Assessment.

5. COURSE DETAILS

Unit	Major Learning Outcomes	Topics and Sub-topics
Unit – I Computer Architecture & Register-Transfer and Micro-operations	1a. Describe different types of Flip Flops.	1.1 Overview of computers and basics of Digital Electronics-Flip Flops, Registers, Shift registers
	1b. Explain registers and register transfers are represented in resister transfer language.	1.2 Register - Transfer-Language 1.3 Register Transfer 1.4 Bus Transfer and Memory Transfer
	1c. Describe various arithmetic micro operations.	1.5 Arithmetic Micro-Operations
	1d. List various logic micro operations.	1.6 Logic micro operations
	1e. List various shift operations and explain arithmetic shift operation.	1.7 Shift Micro operation. 1.8 Arithmetic Logic Shift Unit
Unit – II Basic Computer Organization	2a. Discuss the various fields of instruction code.	2.1 Instruction Codes
	2b. Define registers and state the role of each register in a basic computer.	2.2 Computer Registers
	2c. List the types of computer instruction format in a basic computer. 2d. Develop a control timing signals diagram for the given instruction.	2.3 Computer Instructions 2.4 Timing and Control
	2e. Explain phases of instruction cycle.	2.5 Instruction Cycle 2.6 Memory Reference Instructions
	2f. Describe interrupt.	2.7 Input-Output and Interrupt

Unit	Major Learning Outcomes	Topics and Sub-topics
	2g. Draw functional block diagram of the hypothetic BASIC computer.	2.8 Complete Computer Description
Unit – III Central processor organization& Pipeline processing	3a. Draw General Register organization.	3.1 General Register Organization
	3b. Define stack. Explain the stack organization of CPU.	3.2 Stack Organization
	3c. Define instruction and instruction format.	3.3 Instruction Formats
	3d. Discuss various addressing modes used in computers.	3.4 Addressing Modes
	3e. Explain data transfer and data manipulation instruction.	3.5 Data Transfer and manipulation:
	3f. Discuss program control instructions.	3.6 Program Control
	3g. Compare RISC and CISC Architecture.	3.7 RISC 3.8 CISC Characteristics 3.9 RISC Characteristics
	3h. Describe pipelining in CPU Design.	3.10 Parallel Processing
Unit – IV Memory Organization	4a. Classify various types of Memory. 4b. Understand memory hierarchy and interleaving.	4.1 Memory classifications 4.2 RAM,ROM,PROM,EPROM 4.3 Memory Hierarchy
	4c. Discuss different types of main memory. 4d. Discuss different types of auxiliary memory.	4.4 Main Memory and Auxiliary Memory
	4e. Define Associative Memory.	4.5 Associative Memory
	4f. Describe cache and virtual memory. 4g. List advantages and disadvantages of using cache memory. 4h. Describe various architectural aids to implement cache and virtual memory.	4.6 Cache Memory 4.7 Virtual memory
Unit – V Input/output Organization	5a. Define I/O interface.	5.1 Input-Output Interface
	5b. Explain methods of Asynchronous Data transfer.	5.2 Asynchronous Data Transfer 5.3 Strobe Control 5.4 Handshaking
	5c. Describe Asynchronous Serial Transfer.	5.5 Asynchronous Serial Transfer
	5d. Name different modes of data transfer.	5.6 Modes of Data Transfer
	5e. Discuss Input Output processor and its organization.	5.7 Input-Output Processor (IOP)

6. SUGGESTED SPECIFICATION TABLE WITH HOURS & MARKS (THEORY)

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Computer Architecture & Register Transfer and Micro-operations	11	7	10	0	17
II	Basic Computer Organization	6	2	7	2	11
III	Central processor organization& Pipeline processing	10	6	8	2	16
IV	Memory Organization	8	5	10	0	15
V	Input/output Organization	7	3	8	0	11
	Total	**42**	**23**	**43**	**4**	**70**

Legends: R = Remembrance; U = Understanding; A = Application and above levels (Revised Bloom's taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

7. SUGGESTED LIST OF EXERCISES/PRACTICALS

The practical/exercises should be properly designed and implemented with an attempt to develop different types of cognitive and practical skills **(Outcomes in cognitive, psychomotor and affective domain)** so that students are able to acquire the competencies.

Following is the list of practical exercises for guidance.

Note*: Here only outcomes in psychomotor domain are listed as practical/exercises. However, if these practical/exercises are completed appropriately, they would also lead to development of* ***Programme Outcomes/Course Outcomes in affective domain*** *as given in a common list at the beginning of curriculum document for this programme. Faculty should refer to that common list and should ensure that students also acquire those Programme Outcomes/Course Outcomes related to affective domain*

S. No.	Unit No.	Practical Exercises (Outcomes' in Psychomotor Domain)	Hrs. required
1	I		02

8. SUGGESTED LIST OF STUDENT ACTIVITIES

Following is the list of proposed student activities like:

Prepare seminars

9. SPECIAL INSTRUCTIONAL STRATEGIES (if any)

10. SUGGESTED LEARNING RESOURCES

A) List of Books

S. No.	Title of Book	Author	Publication
1.	Computer system Architecture	Mano ,M. Morris	Pearson publication, Latest Edition ISBN**:** 978-81-317-0070-9
2.	Computer Architecture and Organization	Ghoshal, Subrata	Pearson publication, Latest Edition
3.	Computer Architecture	Parhami, Behrooz	Oxford publication, Latest Edition ISBN: 978-0-19-808407-5

B) List of Major Equipment/ Instrument with Broad Specifications

C) List of Software/Learning Websites

1. http://www.ddegjust.ac.in/studymaterial/msc-cs/ms-07.pdf
2. http://www.iitg.ernet.in/asahu/cs222/Lects/
3. http://www.srmuniv.ac.in/downloads/computer_architecture.pdf

11. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- Prof. R. M. Shaikh, H.O.D Computer Department, K. D. Polytechnic, Patan
- Prof. K. N. Raval, H.O.D Computer Department, R. C. Technical Institute, Ahmedabad
- Prof. R. K. Vaghela, Lecturer Computer Department, R. C. Technical Institute, Ahmedabad

Coordinator and Faculty Members from NITTTR Bhopal

- Prof. (Mrs.) Susan S. Mathew
- Dr. Joshua Earnest,